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SCB12Q4G160AF-07QI

4Gbit DDR4 SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. A

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2021-04	A	Initial Release

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Contents

1 Features

The 4Gbit DDR4 SDRAM offers the following key features:

- Power supply
  - VDD = VDDQ = 1.2V ± 5%
  - VPP = 2.5V -5% + 10%
- Data rate
  - 2666Mbps (DDR4-2666)
- Package
  - 96-ball FBGA
  - Lead-free
- 8 internal banks
  2 groups of 4 banks each (x16)
- Differential clock inputs operation
  (CK_t and CK_c)
- Bi-directional differential data strobe
  (DQS_t and DQS_c)
- Asynchronous reset is supported
  (RESET_n)
- ZQ calibration for Output driver by compare to external reference resistance
  (RZQ 240 ohm 1%)
- Nominal, park and dynamic On-die Termination
  (ODT)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge
- CAS Latency (CL): 9, 10, 11, 12, 13, 14, 15, 16, 17,18, 19, 20, 21, 22 and 23 supported
- Additive Latency (AL) 0, CL-1, and CL-2 supported
- Burst Length (BL): 8 and 4 with on the fly supported
- CAS Write Latency (CWL): 9, 10, 11, 12, 14, 16 and 18 supported
- Operating case temperature range TC = -40℃ to +95℃
- Refresh cycles

Average refresh period 7.8μs at 0℃ TC +85℃
3.9μs at +85℃ < TC +95℃

- Fine granularity refresh is supported
- Adjustable internal generation VREFDQ
- Pseudo Open Drain (POD) interface for data input/output
- Driver strength selected by MRS
- The high-speed data transfer by the 8 bits pre-fetch
- Temperature Controlled Refresh (TCR) mode is supported
- Low Power Auto Self Refresh (LPASR) mode is supported
- Self refresh abort is supported
- Programmable preamble is supported
- Write leveling is supported
- Command/Address latency (CAL) is supported
- Multipurpose register READ and WRITE capability
- Command Address Parity (CA Parity) for command address signal error detect and inform it to controller
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation
- Data Bus Inversion (DBI) for Improve the power consumption and signal integrity of the memory interface
- Data mask (DM) for write data
- Per DRAM Addressability (PDA) for each DRAM can be set a different mode register value individually and has individual adjustment
- Gear down mode (1/2 and 1/4 rate) is supported
- PPR and sPPR is supported
- Connectivity test (x16 only)
- Maximum power down mode for the lowest power consumption with no internal refresh activity
- JEDEC JESD-79-4 compliant

2 Product List

Table 1 shows all possible products within the 4Gbit DDR4 SDRAM component generation.

Table 1 - Ordering Information for 4Gbit DDR4 Component

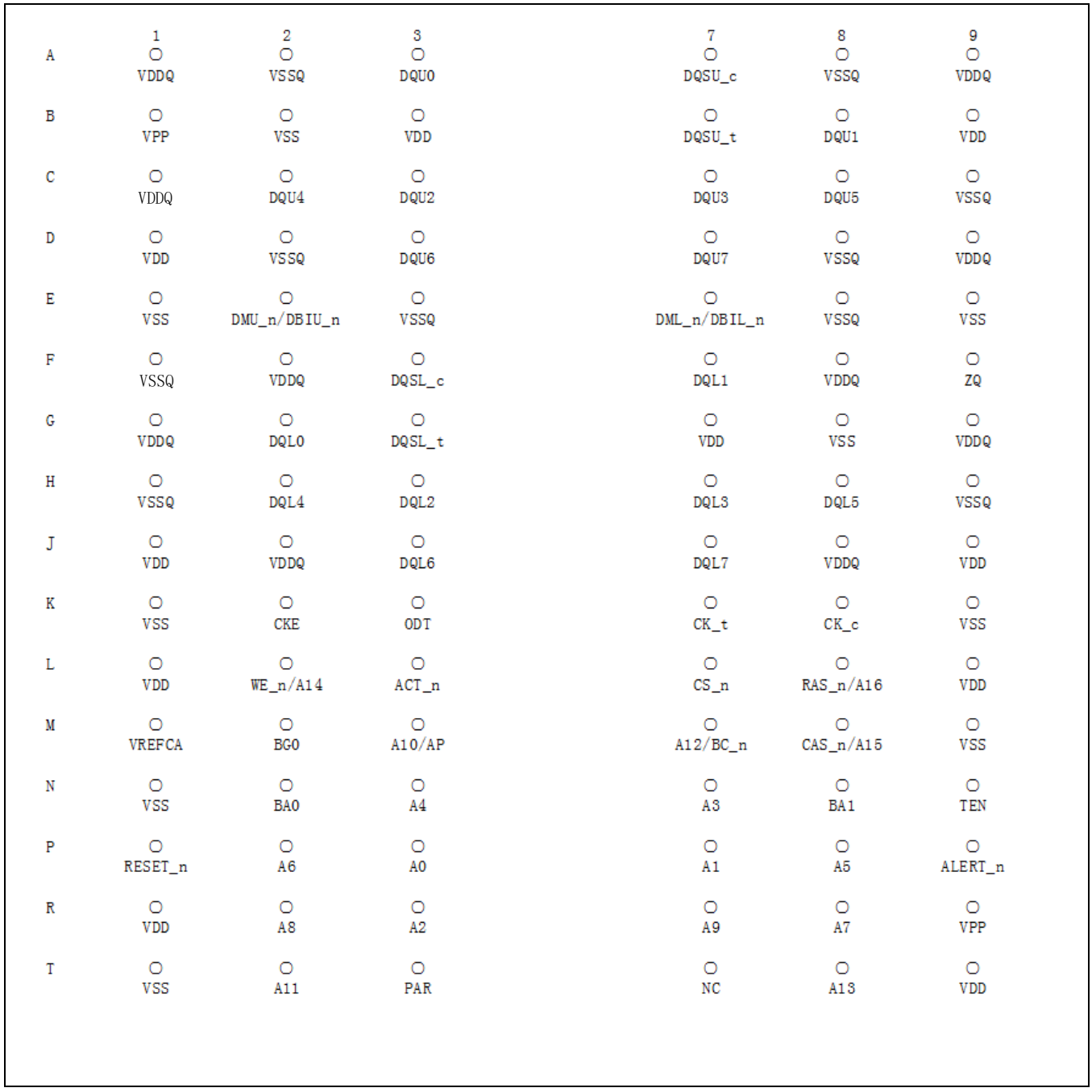
UniIC Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Speed Sort Name	Package
4Gbit DDR4 SDRAM Components in × 16 Organization (256 M × 16)				
SCB12Q4G160AF-07QI	1333 MHz	19-19-19	DDR4–2666V	PG-FBGA-96

Table 2 - 4Gbit DDR4 Addressing

Parameter	256Mb × 16	Note
Number of bank groups	2	
Bank group address	BG0	
Bank count per group	4	
Bank address in bank group	BA[1:0]	
Row Address	32K (A[14:0])	
Column Address	1K(A[9:0])	
Page Size	2KB	

3 Ball configuration

Figure 1 - Ball out for 256Mb ×16 Components (96-ball FBGA)



	1	2	3	7	8	9
A	VDDQ	VSSQ	DQU0	DQSU_c	VSSQ	VDDQ
B	VPP	VSS	VDD	DQSU_t	DQU1	VDD
C	VDDQ	DQU4	DQU2	DQU3	DQU5	VSSQ
D	VDD	VSSQ	DQU6	DQU7	VSSQ	VDDQ
E	VSS	DMU_n/DBIU_n	VSSQ	DML_n/DBIL_n	VSSQ	VSS
F	VSSQ	VDDQ	DQSL_c	DQL1	VDDQ	ZQ
G	VDDQ	DQL0	DQSL_t	VDD	VSS	VDDQ
H	VSSQ	DQL4	DQL2	DQL3	DQL5	VSSQ
J	VDD	VDDQ	DQL6	DQL7	VDDQ	VDD
K	VSS	CKE	ODT	CK_t	CK_c	VSS
L	VDD	WE_n/A14	ACT_n	CS_n	RAS_n/A16	VDD
M	VREFCA	BG0	A10/AP	A12/BC_n	CAS_n/A15	VSS
N	VSS	BA0	A4	A3	BA1	TEN
P	RESET_n	A6	A0	A1	A5	ALERT_n
R	VDD	A8	A2	A9	A7	VPP
T	VSS	A11	PAR	NC	A13	VDD

4 Ball Description

Table 3 - Input / Output Signal Functional Description for 256Mb ×16 Components (96-ball FBGA)

Ball Name	Function	Note
A0 to A14	Address inputs A10/AP: Auto precharge A12/BC_n: Burst chop	2
BA0, BA1	Bank select	2
BG0	Bank group input	2
DQU0 to DQU7 DQL0 to DQL7	Data input/output	
DQSU, DQSU_n DQSL, DQSL_n	Differential data strobe	
CS_n	Chip select	2
RAS_n/A16 CAS_n/A15 WE_n/A14	Command input	2
ACT_n	Activation command input	2
CKE	Clock enable	2
CK_t, CK_c	Differential clock input	
DMU_n, DML_n	Write data mask	
DBIU_n, DBIL_n	Data bus inversion	
ODT	ODT control	2
RESET_n	Active low asynchronous reset	2
PAR	Command and address parity	
ALERT_n	Alert	
TEN	Connectivity test mode enable	
VDD	Supply voltage for internal circuit	
VSS	Ground for internal circuit	
VDDQ	Supply voltage for DQ circuit	
VSSQ	Ground for DQ circuit	
VREFCA	Reference voltage for CA	
ZQ	Reference pin for ZQ calibration	
NC	No connection	1

Note:
1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination.

5 Electrical Specifications

Table 4 - IDD & IDDQ Specification

Symbol	x16	Unit
I_{DD0}	92	mA
I_{DD0A}	93	mA
I_{DD1}	142	mA
I_{DD1A}	146	mA
I_{DD2N}	74	mA
I_{DD2NA}	75	mA
I_{DD2NT}	97	mA
I_{DD2NL}	63	mA
I_{DD2NG}	71	mA
I_{DD2ND}	52	mA
I_{DD2N_par}	94	mA
I_{DD2P}	44	mA
I_{DD2Q}	75	mA
I_{DD3N}	86	mA
I_{DD3NA}	85	mA
I_{DD3P}	67	mA
I_{DD4R}	205	mA
I_{DD4RA}	227	mA
I_{DD4RB}	206	mA
I_{DD4W}	230	mA
I_{DD4WA}	266	mA
I_{DD4WB}	215	mA
I_{DD4WC}	210	mA
I_{DD4W_par}	204	mA
I_{DD5B}	180	mA
I_{DD5F2}	189	mA
I_{DD5F4}	160	mA
I_{DD7}	235	mA
I_{DD8}	30	mA

Table 5 - IPP Specification

Symbol	X16	Unit
IPP0	9	mA
IPP1	9	mA
IPP2N	7	mA
IPP2P	7	mA
IPP3N	7	mA
IPP3P	7	mA
IPP4R	7	mA
IPP4W	7	mA
IPP5B	27	mA
IPP5F2	29	mA
IPP5F4	20	mA
IPP7	40	mA
IPP8	3	mA

Table 6 - IDD6 Specification

Symbol	Temperature Range	DDR4-2666		Unit	Notes
		IDD(max)	IPP(max)		
IDD6N	-40 - 85 ^{o}C	30	6	mA	1
IDD6E	-40 - 95 ^{o}C	36	8	mA	2
IDD6R	-40- 45 ^{o}C	25	4	mA	3
IDD6A	-40 - 85 ^{o}C	30	6	mA	4

Note:
1. Applicable for MR2 settings A6 = 0 and A7 = 0.
2. Applicable for MR2 settings A6 = 0 and A7 = 1. IDD6E is only specified for devices which support the extended temperature range feature.
3. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6R is only specified for devices which support the reduced temperature range feature.
4. Applicable for MR2 settings A6 = 1 and A7 = 1. IDD6A is only specified for devices which support the auto self-refresh feature.

6 Speed Bin

Table 7 - DDR4-2666 Speed Bins

Speed Bin				DDR4-2666V		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal read command to first data			tAA	14.25[14] (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.25 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	13
Supported CL Settings with read DBI				12,(13),14,(15),16,(18),19,(20),21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

Note:
Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400 and 2666 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 , 0.833 or 0.750 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA
= 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns or 0.750 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Reserved for DDR4-3200 speed bin.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameter apply from tCK(avg)min to tCH(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

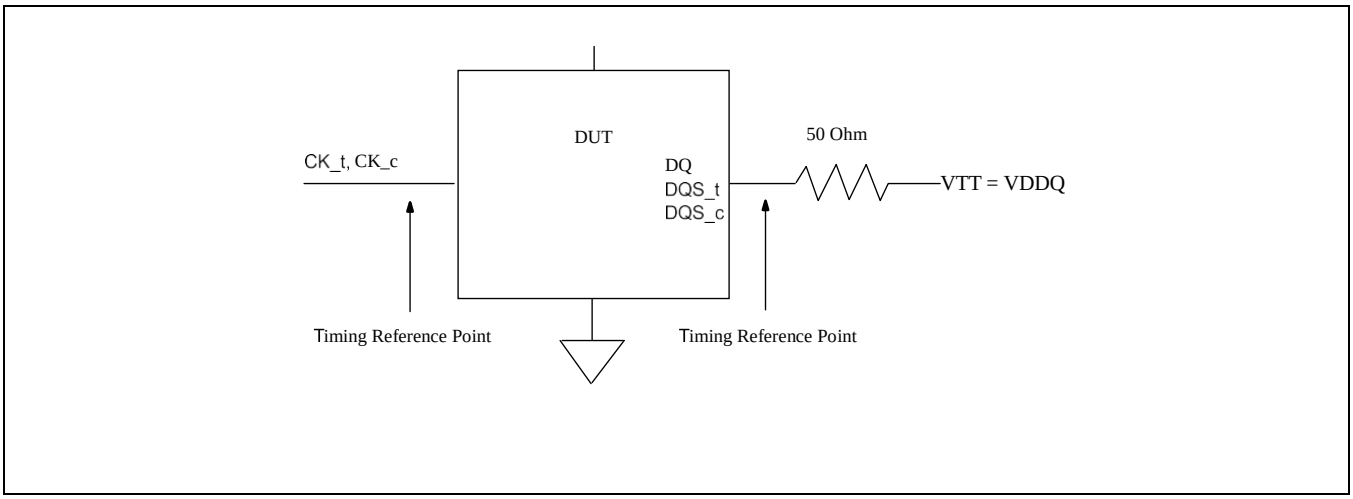
7 Electrical Characteristics & Timing

7.1 Reference Load for AC Timing and Output Slew Rate

Figure 2 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 2 - Reference Load for AC Timings and Output Slew Rates



7.2 Timing Parameters by Speed Grade

Table 8 - AC Timing parameters for DDR4-2666

Speed		DDR4-2666		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns	
Average Clock Period	tCK(avg)	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-38	38	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_to- tal	75		ps	25
Cycle to Cycle Period Jitter determin- istic	tJIT(cc)_dj	38		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	60		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-101	101	ps	
Cumulative error across 13 cycles	tERR(13per)	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)		ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	55	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	145	-	ps	
Command and Address hold timeto CK_t, CK_c referenced to Vih(dc) /Vil(dc) levels	tIH(base)	80	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	145	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	ps	
Command and Address Timing					
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 5.000ns)	-	nCK	34

Speed		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX		
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1KB page size	tRRD_S(1K)	Max(4nCK, 3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK, 3 ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 12ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	ns	1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	ns	1,34
Internal READ Command to PRE- CHARGE Command delay	tRTP	Max(4nCK, 7.5ns)	-	ns	34
WRITE recovery time	tWR	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK, 3.75ns)	-	ns	1, 28
delay from start of internal write trans- action to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK, 3.75ns)	-	ns	2, 29, 34
delay from start of internal write trans- action to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK, 3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	854	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	nCK	37
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK	33
Multi Purpose Register Write Recov- ery Time	tWR_MPR	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + pre- charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK	
CS_n to Command Address Latency					
CS_n to Command Address Latency	tCAL	5	-	nCK	
DRAM Data Timing					
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	tCK(avg) /2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.74	-	tCK(avg) /2	13,17, 18

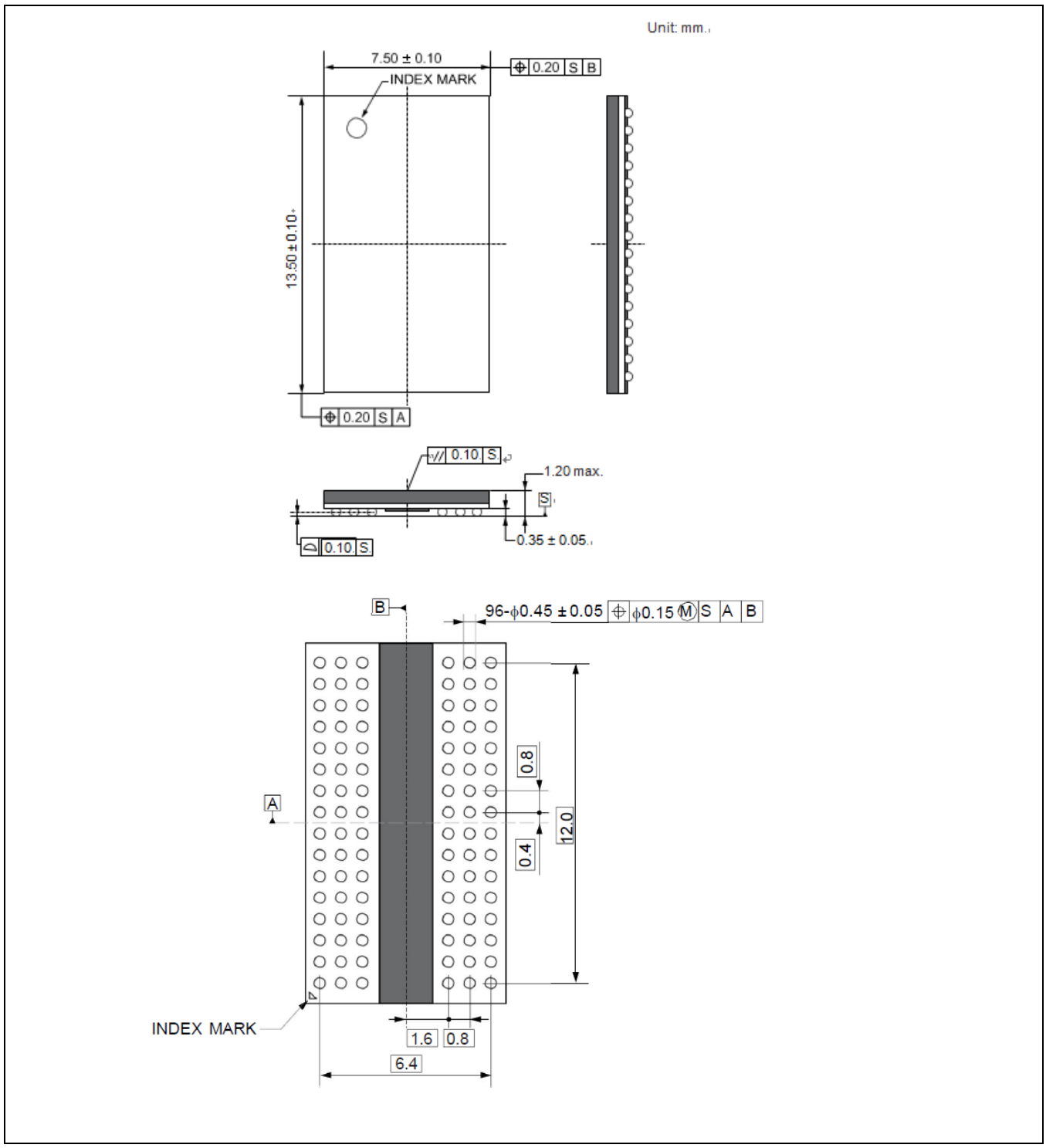
Speed		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX		
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	-	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE2	1.8	-	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK	21
DQS_t,DQS_c differential outputlow time	tQSL	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Preamble(2 clock preamble)	tWPRE2	1.8	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-170	170	ps	
MPSM Timing					
Command path disable delay upon MPSM entry	tMPED	tMOD (MIN) + tCPDED (MIN)	-	nCK	
Valid clock requirement after MPSM entry	tCKMPE	tMOD (MIN) + tCPDED (MIN)	-	nCK	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (MIN)	-	nCK	
Exit MPSM to commands not requir- ing a locked DLL	tXMP	tXS (MIN)	-	nCK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP (MIN) + tXSDLL (MIN)	-	nCK	
CS setup time to CKE	tMPX_S	tIS (MIN) + tIH (MIN)	-	ns	
CS_n High hold time to CKE rising edge	tMPX_HH	tXP	-	ns	
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	ns	
Calibration Timing					
Power-up and RESET calibration time	tZQinit	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	nCK	
Reset/Self Refresh Timing					
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)		nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self RefreshABORT	tX- S_ABORT(min)	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to commands re- quiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK	
Minimum CKE low width for Self re- fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	nCK	
Minimum CKE low width for Self re- fresh entry to exit timing with CA Par- ity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	nCK	

Note:

1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on the-fly: Rising clock edge 4 clock cycles after WL.
   For BC4 (on the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TCASE
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM\[nCK]=RU{tPARAM\[ns]/tCK(avg)\[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total i ncludes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock.(output deratings are relative to the SDRAM input clock).Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_tDQS_c, as measured from on falling edge to the next.
21. tQSH describes the instantaneous differential output high pulse width on DQS_t DQS_c, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI.
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. T his parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWT
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed Bin Tables shown in section 10.
36. DDR4 1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2
37. For MR7 commands, the minimum delay to a subsequent non -MRS command is 5nCK.

8 Package Outlines

Figure 3 - Package outline(96ball FBGA)



9 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter

Table 9 - DDR4 Memory Components

Field	Description	Values	Coding
1	UniIC Component Prefix	SCB	UniIC
2	Voltage	12	VDD, VDDQ=1.14V-1.26V
3	DRAM Technology	Q	DDR4
4	Density	4G	4 Gbit
5	Number of I/Os	80	X8
		16	X16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
8	Package,	F	FBGA Green
9	Power	–	Standard power product
		L	Low power product
10	Speed Grade	07Q	CL–tRCD–tRP =19-19-19

List of Figures

List of Tables

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